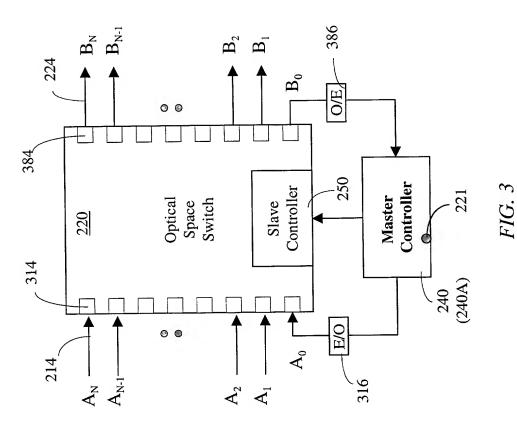
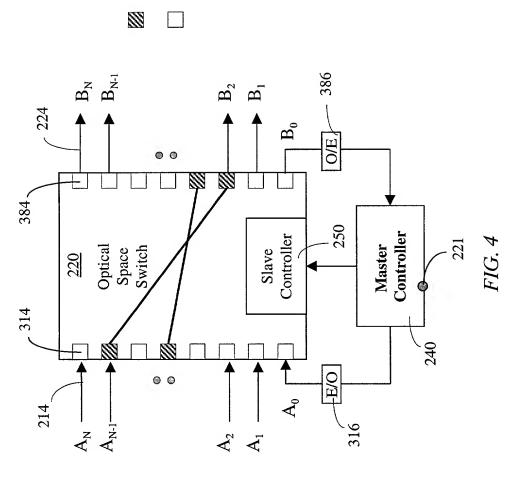


FIG. 2





Channel switched

Burst switches

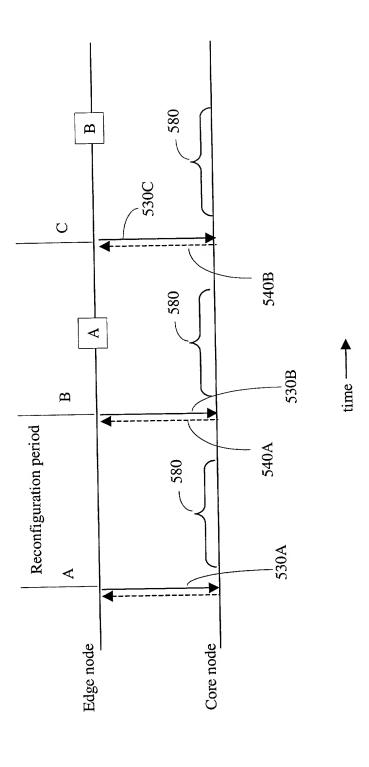
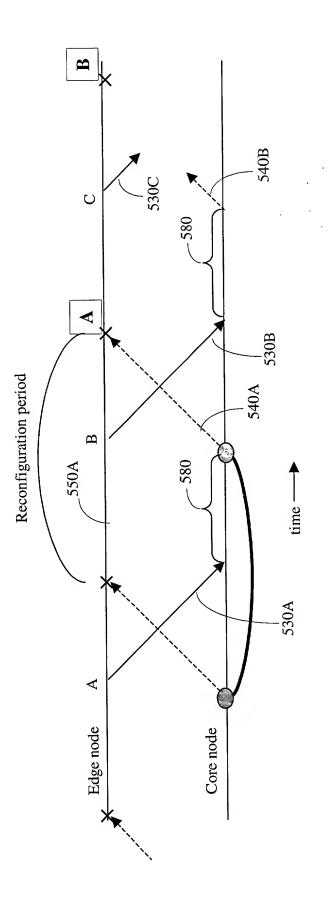


FIG.



FIG

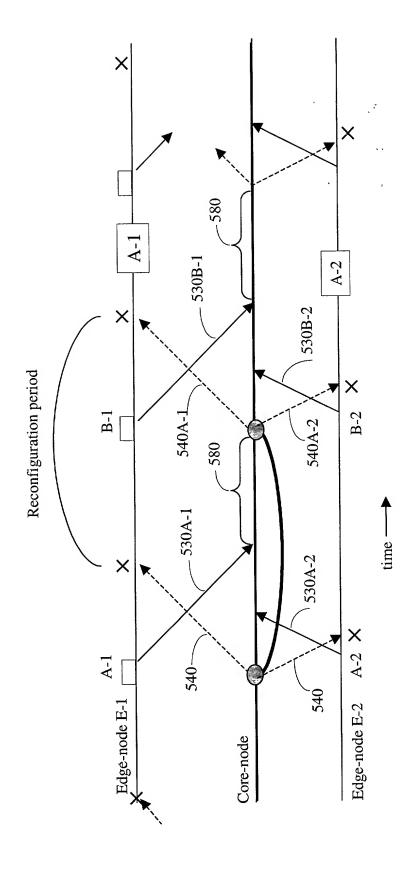
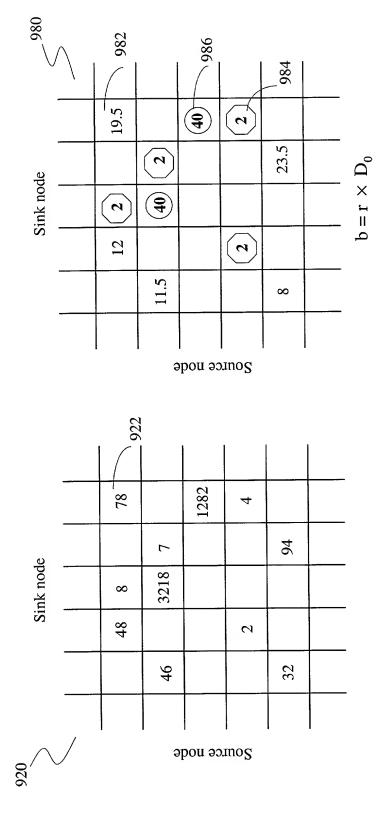
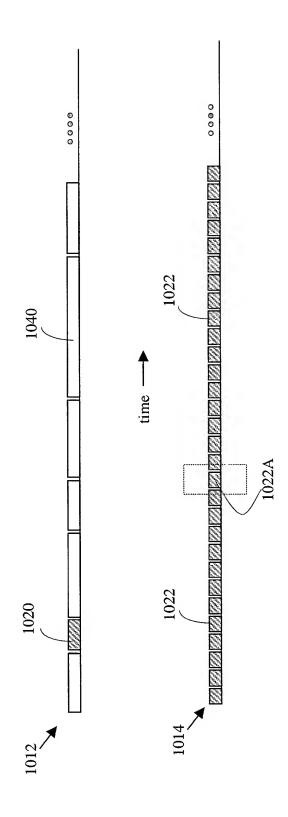
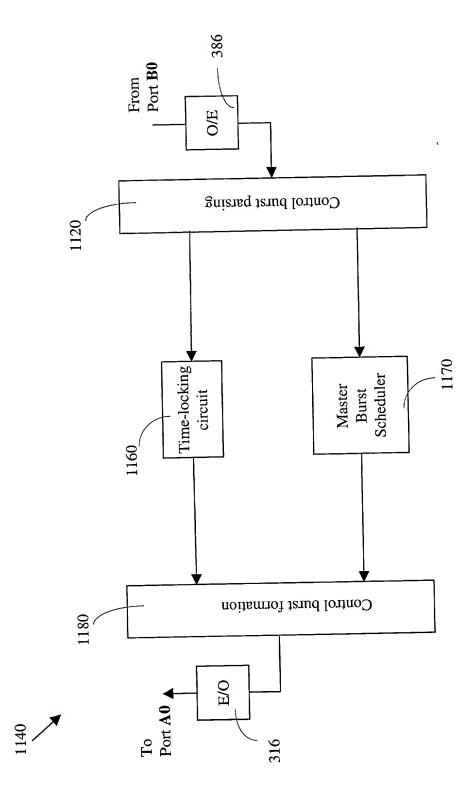


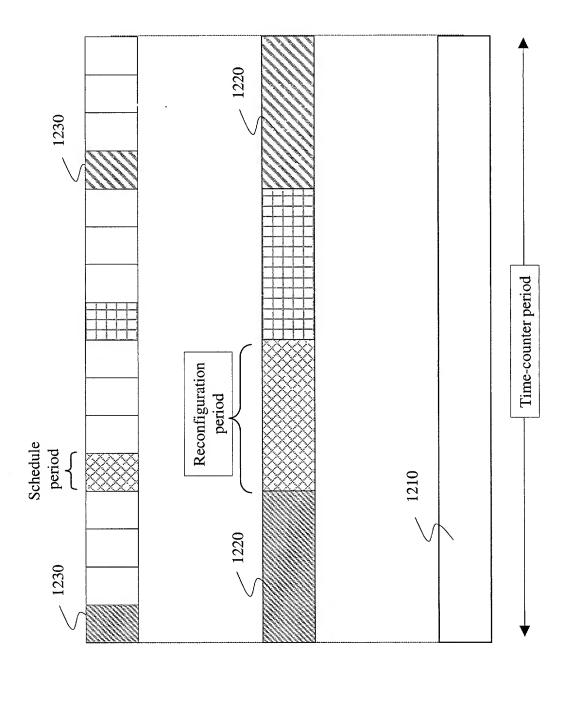
FIG. 7





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INCIPATIO IN INTENT

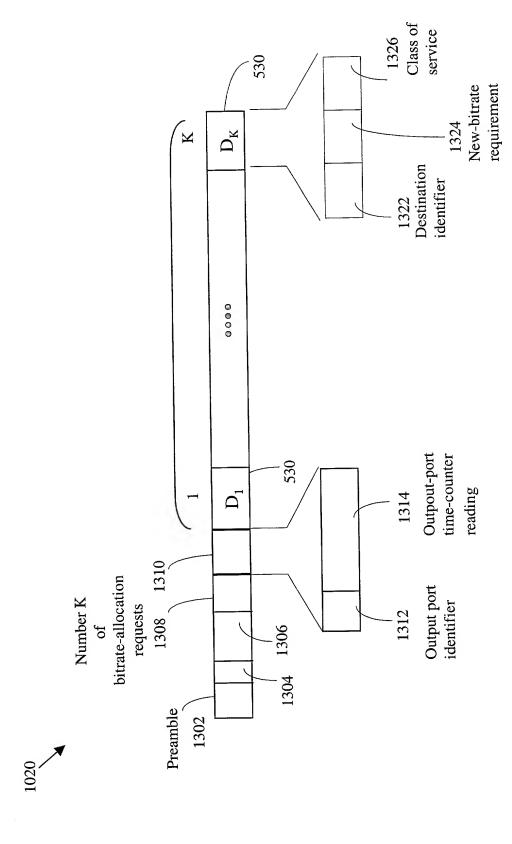
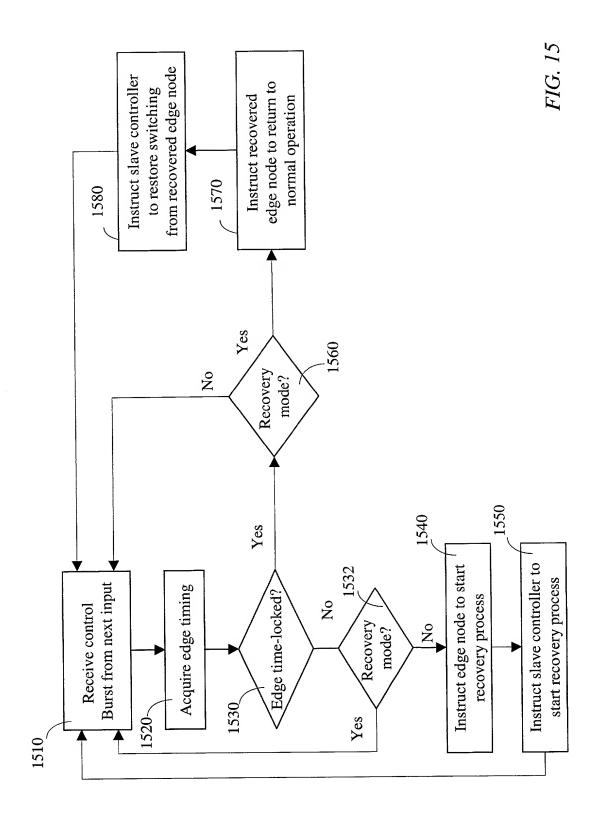
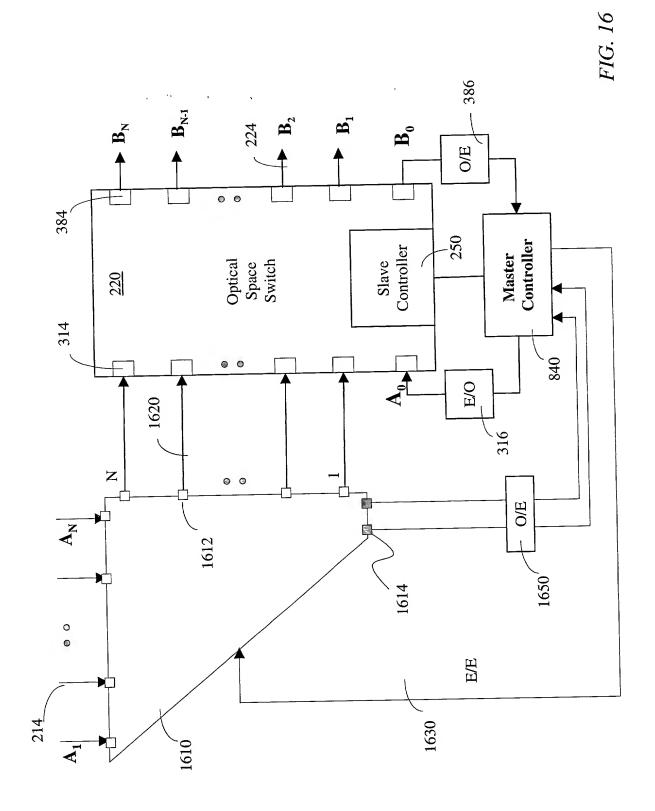
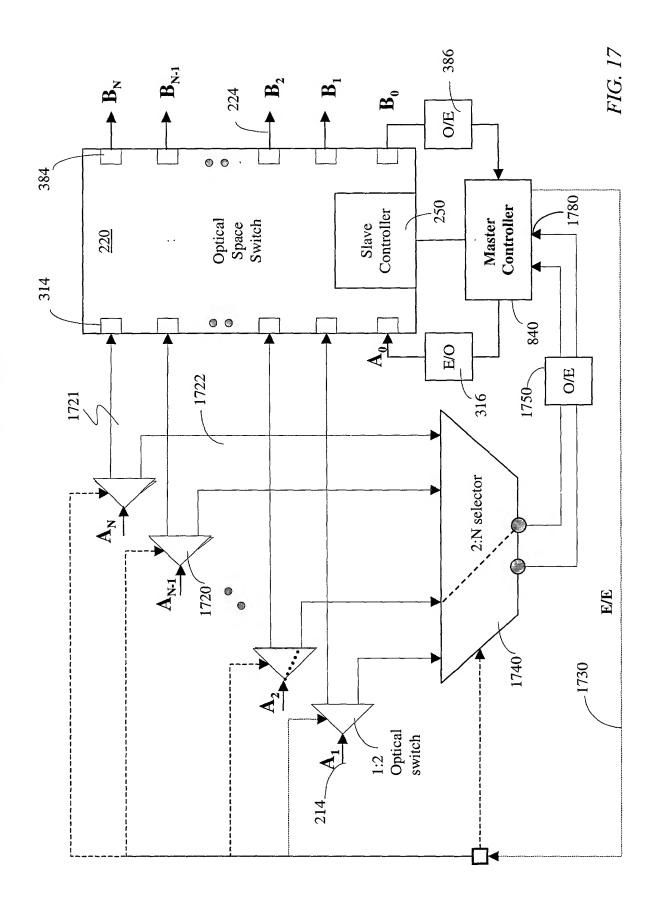
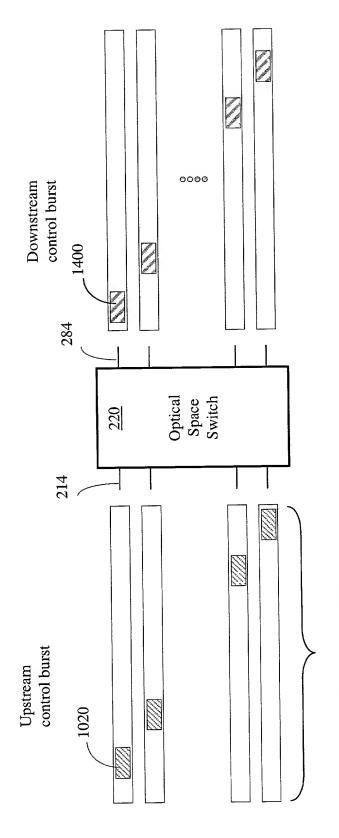


FIG. 14









Reconfiguration period

 $2^{W}-1$ $2^{V}-1$ $|2^{V}-1|$ First schedule period of next master cycle First schedule period of a master cycle Schedule period 2^{V} time slots 0 24 0 $2 \times 2^{\dot{V}}$ $5 \times 2^{\circ}$

Time-counter cycle (master cycle) Period: 2^W time slots



TOUSHSIE IIIIS

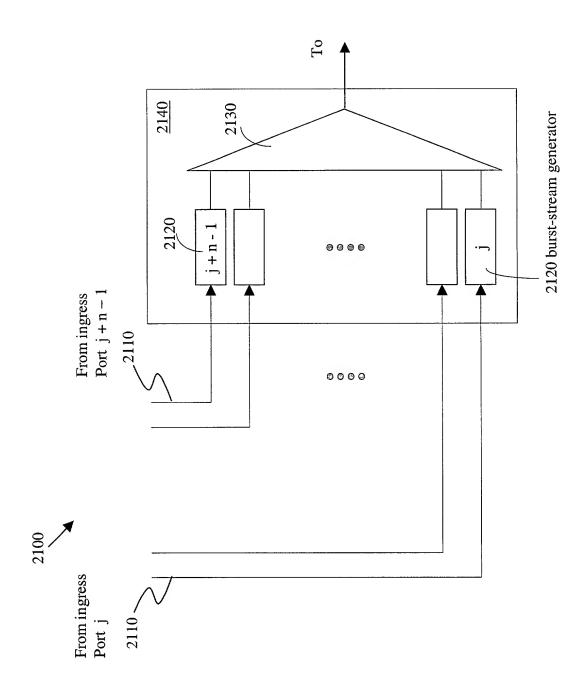
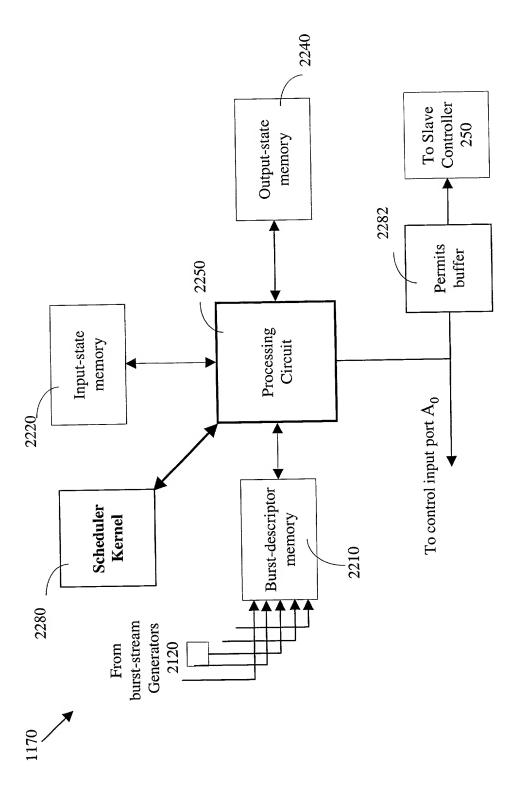
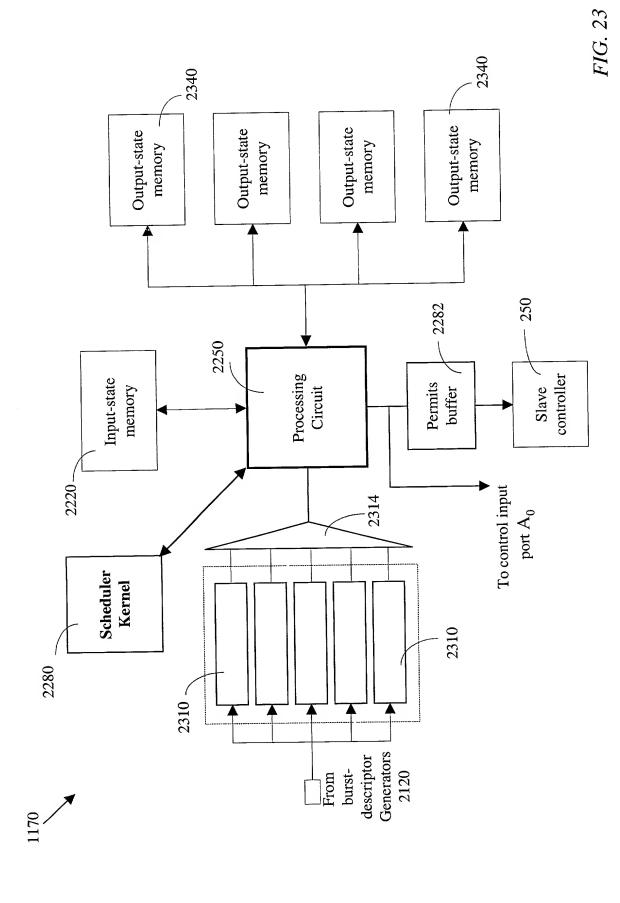
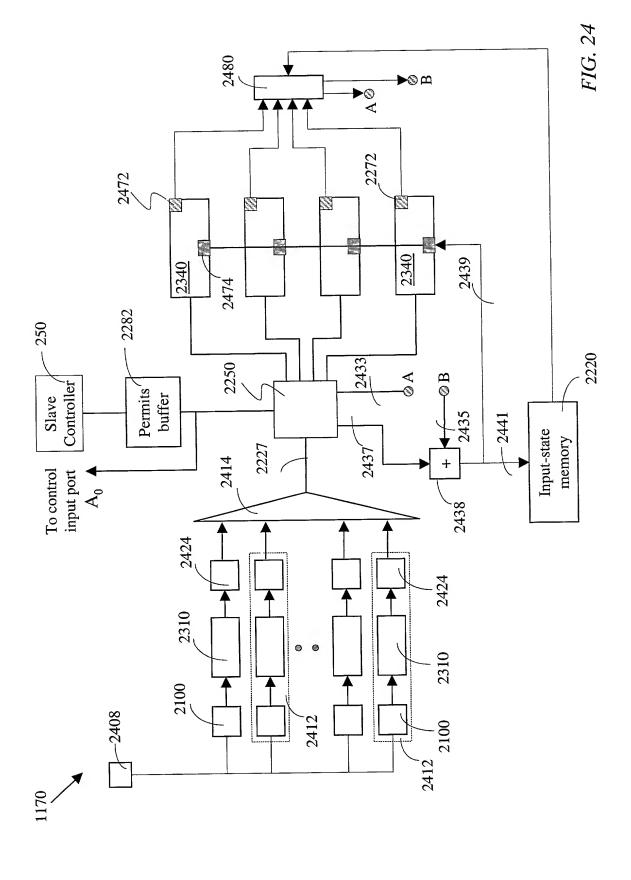


FIG. 2.



INCIPATE IIIII





INDESSIO IN INTERIOR

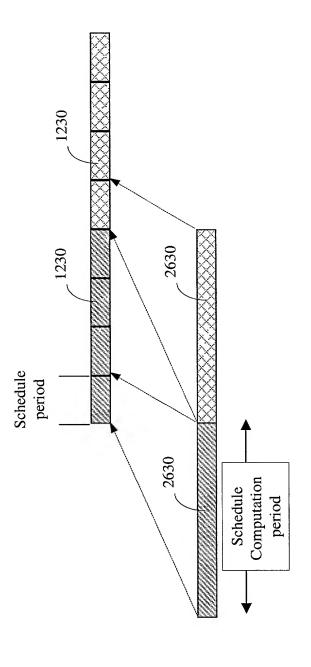
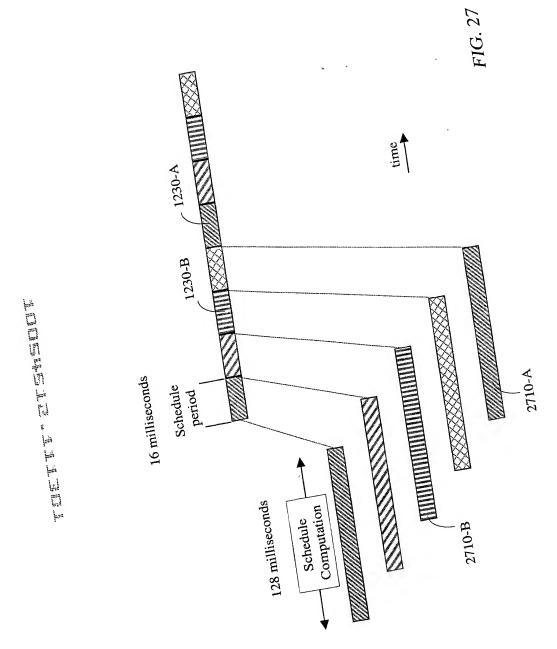


FIG. 26



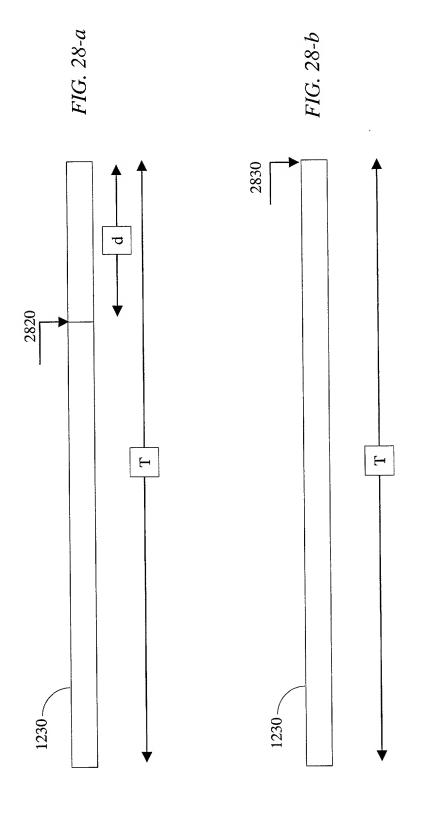
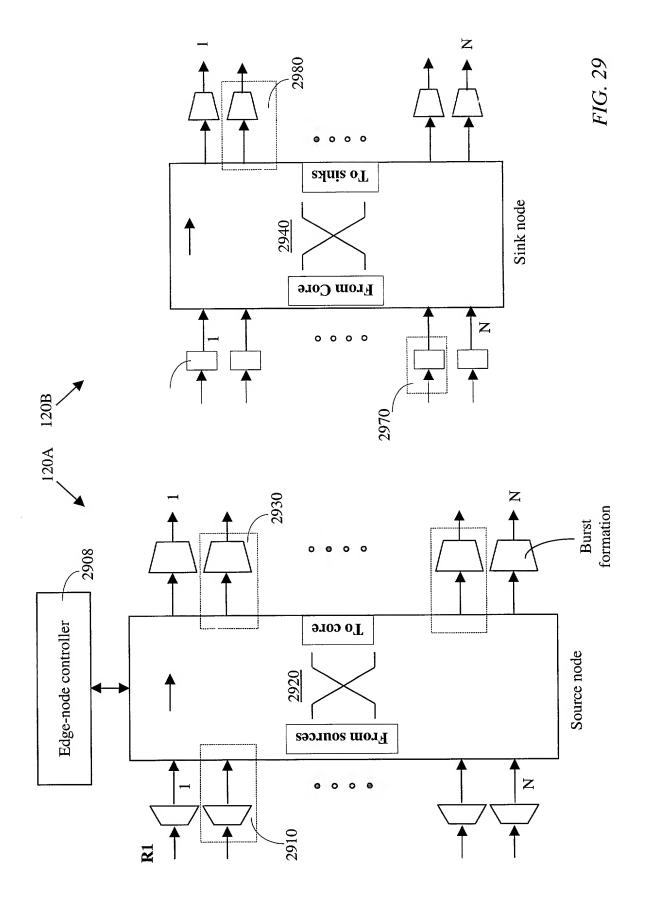


FIG. 28



· >.

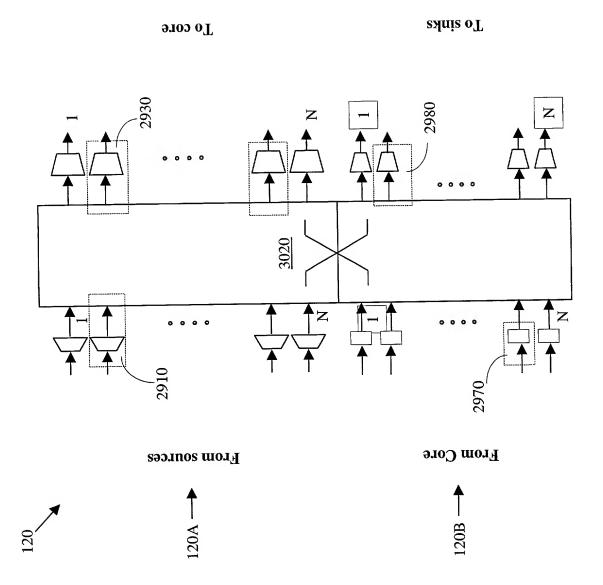
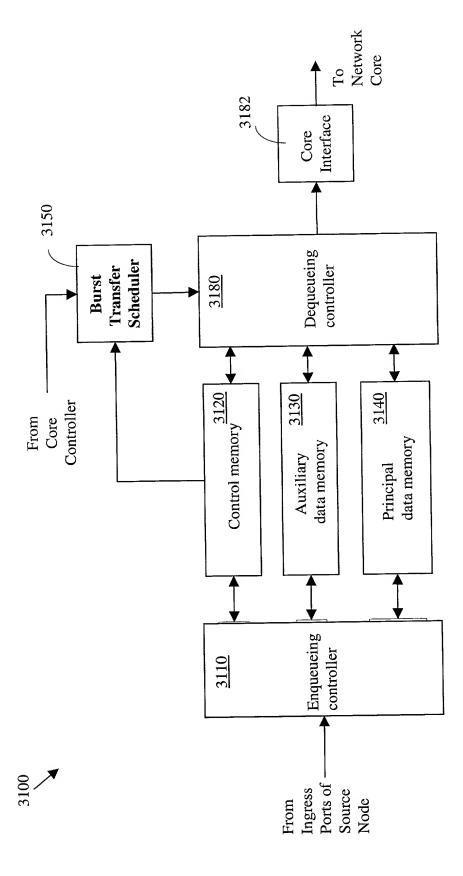
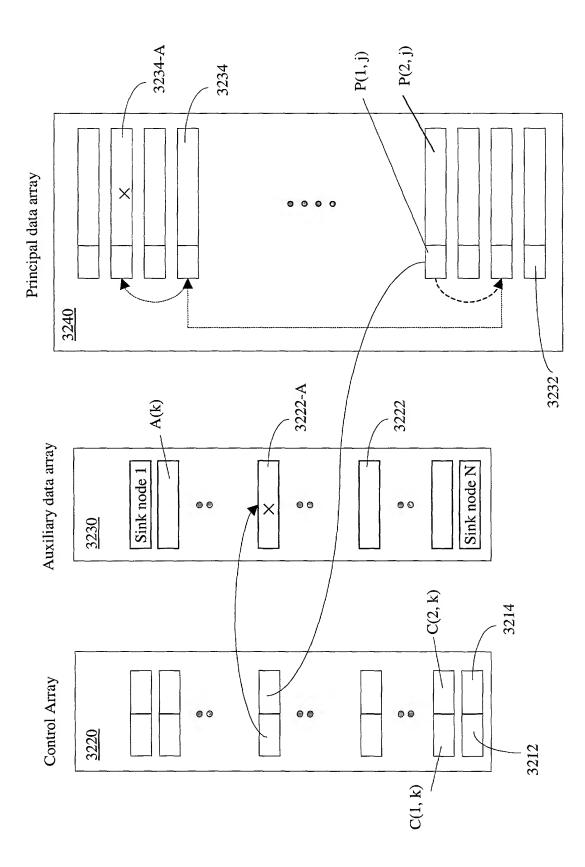
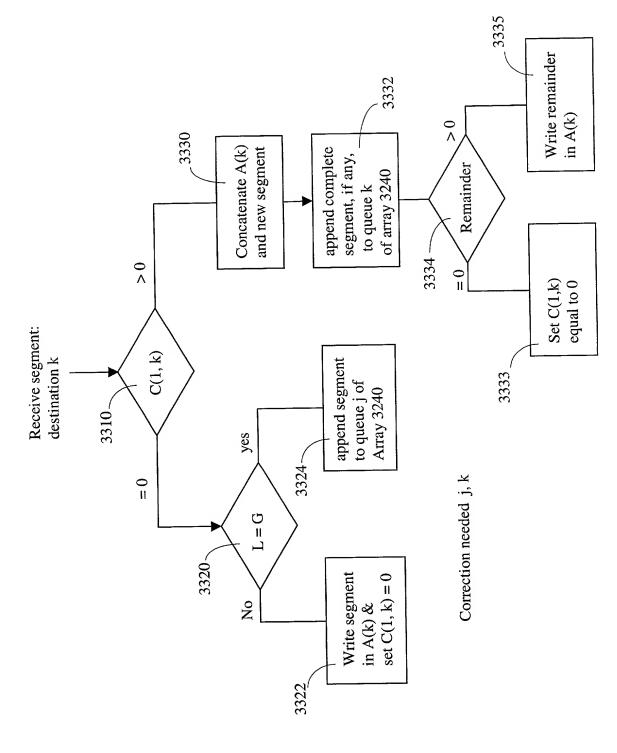


FIG. 30



A CONTRACTOR AND A SCHOOL





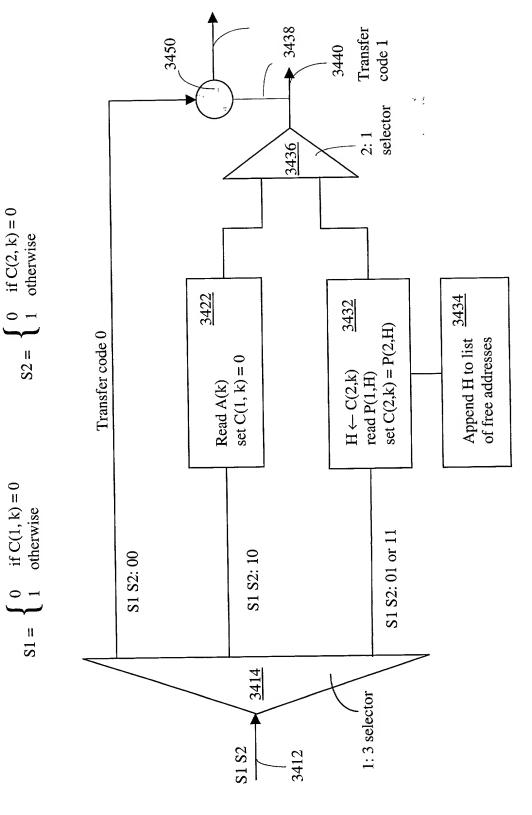


FIG 3/

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